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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/001,961	12/05/2001	Jason G. Sandri	2207/12035	1389

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EXAMINER	
TRUONG, CAMQUY	

ART UNIT	PAPER NUMBER
2127	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/001,961	SANDRI ET AL.	
	Examiner	Art Unit	
	Camquy Truong	2127	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-17 are presented for examination.

2. It is noted that although the present application does contain line numbers in the specification and claims, the line numbers in the claims do not correspond to the preferred format. The preferred format is to number each line of every claim, with each claim beginning with line 1. For ease of reference by both the examiner and Applicant all future correspondence should include the recommended line numbering.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

4. Claims 1-9, 13-15 are rejected under 35 U.S.C 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A. The claim language in the following claims is not clearly understood:

i. As to claim 1, line 3, it is unclear who perform the "obtaining exclusive access" step (i.e. a plurality of logical processors or a first logical processor); line 5, it is unclear who

perform " querying " step (i.e. the first logical processor); lines 7-9, it is not clearly understood what happen after resource descriptor reserve resources for exclusive use by the first logical processor (i.e. waiting or release); line 10, it is unclear when and how the " releasing " step is perform and who perform this step (i.e. not using or else?).

ii. As to claims 2 and 4, lines 2-3, it is unclear who perform the " releasing " step (i.e. first logical processor?).

iii. As to claims 6 and 13, they have the same problems as claim 1 above.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable Hays, Jr. et al. (U.S. Patent 4,354,227).

7. As to claim 1, Hays teaches the invention substantially as claimed including: a method for controlling access to resources shared among a plurality of processors (1-2, Fig.1; col.1, lines 60-67), comprising

Obtaining exclusive access for a first processor to a resource descriptor describing a usage allocation of said shared resources (col.2, lines 9-12; col.10, lines 10-13 and 16-19);

Query resource descriptor to determine whether resources needed by said first processor is available (col.4, lines 24-27; col.5, lines 32-35; col. 10, lines 20-21);

If resources needed by said first processor are available, updating said resource descriptor to reserve said resources for exclusive use by said first processor (col. 5, lines 35-36; col. 6, lines 3-6; col. 10, lines 22-27); and

Releasing said exclusive access for said first processor to said resource descriptor (col. 10, lines 29-45).

8. Hays does not explicitly teach that processors are logical processors. However, Hays disclosed typical microprocessor (col. 9, line 29). It would have been obvious to one of ordinary skill in the art at the time the invention was made to recognize that logical processors are included in the typical microprocessor.

9. As to claim 2, Hays teaches if said resources needed by said first logical processor are not available, releasing said exclusive access for said first logical processor to said resource descriptor (col.5, lines 57-66).

10. As to claim 3, Hays teaches after the releasing, accessing a shared resource by said first logical processor (col. 10, lines 39-45).

11. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable Hays, Jr. et al. (U.S.Patent 4,354,227) as applied to claim 1 above, in view of Scalzi (U.S. Patent 5,895,492).

12. As to claim 4, Hays teaches:

Obtaining access for a second processor to a resource descriptor describing a usage allocation of said shared resources (col.2, lines 9-12; col.10, lines 10-13 and 16-19);

Query resource descriptor to determine whether resources needed by said second logical processor is available (col.4, lines 24-27; col.5, lines 32-35; col. 10, lines 20-21);

If resources needed by said second processor are available, updating said resource descriptor to reserve said resources for exclusive use by said second processor (col. 5, lines 35-36; col. 6, lines 3-6; col. 10, lines 22-27); and

Releasing said exclusive access for said second processor to said resource descriptor (col. 10, lines 29-45).

13. Hays does not explicitly teaches obtaining exclusive access for a second processor to said resources descriptor after exclusive access for the first processor to said resources descriptor is released. However, Scalzi teaches obtaining exclusive access for a second processor to said resources descriptor after exclusive access for the first processor to said resources descriptor is released (col. 3, lines 48-55).

14. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Hays and Scalzi because Scalzi's exclusive access by the second processors after exclusive access by the first processor to said resource descriptor is released, would improve the integrity of Hay's system by providing serialize access to shared resources.

15. As to claim 5, Hays teaches if said resources needed by said second logical processor are not available, releasing said exclusive access for said second logical processor to said resource descriptor (col.5, lines 57-66).

16. Claims 6-12 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable Hays, Jr. et al. (U.S. Patent 4,354,227) in view of DeKoning et al (U.S. Patent 6,823,472 B1).

17. As to claim 6, Hays teaches the invention substantially as claimed including: a method for controlling access to resources shared among a plurality of processors (1-2, Fig.1; col.1, lines 60-67), comprising

Writing to said resource descriptor register to reserve at least a first resource of said plurality of shared resources for exclusive use by said first logical processor (col. 5, lines 35-36; col. 6, lines 3-6; col. 10, lines 22-27).

18. Hays does not explicitly teach that writing to a semaphore register to reserve access by a first logical processor to a resource descriptor register and writing to semaphore register to release said exclusive access by said first logical processor. However, DeKoning teaches writing to a semaphore register to reserve access by a first logical processor to a resource descriptor register (col. 6, lines 13-18) and writing to semaphore register to release said exclusive access by said first logical processor (col. 6, lines 43-47).

19. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Hays and DeKoning because DeKoning's writing to a semaphore register to reserve/ release access by a first

logical processor to a resource descriptor register would improve the book keeping of resources for a multiprocessor system by explicitly having the processor to write to the register when reserve/release the reasources.

20. As to claim 7, it is rejected for the same reason as claim 6. In addition, Hays teaches the second processor (1-2, Microprocessor A, Microprocessor B, Fig.1).

21. As to claim 8, Hays teaches resource descriptor register comprises at least one logical processor identifier associated with one of said first and second logical processors (col. 2, lines 20-21; col. 6, line 66-col.7, line 4).

22. As to claim 9, Hays teaches said resource descriptor register further comprises a status identifier associated with said logical processor identifier (col. 2, lines 20-23; col. 6, lines 3-11).

23. As to claim 10, Hays teaches:

A plurality of logical processors (1-2, Multiprocessor A, Multiprocessor B, Fig.1, col. 1, line 64);

A plurality of resources shared by said plurality of logical processors (col. 1, lines 59-64);

A resource descriptor to identify a status of said shared resources (col. 10, lines 9-13); and

A semaphore to control access by said plurality of logical processors to said resource descriptor (col. 2, lines 8-12; col. 10, lines 16-19).

24. As to claim 11, it is rejected for the same reason as claim 6.

25. As to claim 12, it is rejected for the same reason as claim 11. In addition, Hays teaches first and second processors concurrently use first and second resources (col. 1, lines 7-16; col. 7, lines 55-61).

26 As to claim 16, it is rejected for the same reason as claim 6. In addition, Hays teaches:

A plurality of processors and plurality of resources shared by said processor (1-2, Multiprocessor A, Multiprocessor B, Fig.1, col. 1, lines 59-64);

A resource descriptor that controls access to said resources (col.2, lines 9-12; col.10, lines 10-13 and 16-19);

A semaphore register that controls access to said resources descriptor (col. 2, lines 8-12; col. 10, lines 16-19);

A semaphore access control hardware that controls access to said semaphore register (col. 2, lines 8-12; col. 10, lines 16-19);

Causing a first logical processor to execute software to supply an identifier of said first logical processor to said semaphore access control hardware (col. 2, lines 20-21); and

27. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable Hays, Jr. et al. (U.S. Patent 4,354,227) in view of Florek (U.S. Patent 6,795,901).

28. As to claim 13,

Hays teaches:

Reserve exclusive access to resource descriptor register (col.2, lines 9-12; col.10, lines 10-13 and 16-19);

Generating a first bitmap identifying said first required resource (col. 5, lines 35-36; col. 6, lines 3-6; col. 10, lines 22-27), and using first resource (col.10, lines 43-45);

Applying said first bitmap to said resources descriptor register to reserve said first require resource (col. 5, lines 35-36; col. 6, lines 3-6; col. 10, lines 22-27).

29. Hays does not explicitly teaches setting a lock bit in a semaphore register and re-setting semaphore lock bit to release exclusive access. However, Florek teaches: setting a lock bit in a semaphore register (col. 10, lines 39-42) and re-setting semaphore lock bit to release exclusive access (col. 10, lines 43-53).

30. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Hays and Florek because Forek's setting a lock bit in a semaphore register and re-setting semaphore lock bit to release exclusive access would provide enhanced performance over standard memory interfaces by permitting the implementation of read-modify-write functionality.

31. As to claim 14, it is rejected for the same reason as claim 13. In addition, Hays teaches first and second processors use first and second resources in parallel (col. 1, lines 7-16; col. 7, lines 55-61).

32. As to claim 15, Hays teaches setting a lock bit comprises supplying an identifier of said first logical processor for writing into said semaphore register (col. 2, lines 20-21; col. 6, lines 3-11; col. 6, line 66-col.7, line 4).

33. Claim 17 are rejected under 35 U.S.C. 103(a) as being unpatentable Hays, Jr. et al. (U.S. Patent 4,354,227) in view of DeKoning et al (U.S. Patent 6,823,472 B1), as apply to claims 6 and 16 above, and further in view of Scalzi et al (U.S. Patent 5,895,494).

34. As to claim 17, it was rejected as claims 6 and 16 above, in additionHays teaches: Causing a first logical processor to execute software to supply an

identifier of said first logical processor to said semaphore access control hardware (col. 2, lines 20-21).

35. Hays does not explicitly teach that writing to a semaphore register to reserve access by a first logical processor to a resource descriptor register and writing to semaphore register to release said exclusive access by said first logical processor. However, DeKoning teaches writing to a semaphore register to reserve access by a first logical processor to a resource descriptor register (col. 6, lines 13-18) and writing to semaphore register to release said exclusive access by said first logical processor (col. 6, lines 43-47).

26. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Hays and DeKoning because DeKoning's writing to a semaphore register to reserve/ release access by a first logical processor to a resource descriptor register would improve the book keeping of resources for a multiprocessor system by explicitly having the processor to write to the register when reserve/release the reasources.

37. Hays and DeKoning do not explicitly teach that detecting said first logical processor has failed. However, Scalzi teaches detecting said first logical processor has failed (col. 4, lines 1-7; col. 7, lines 42-44; col. 8, lines 9-14).

38. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Hays, DeKoning and Scalzi because Scalsi's detecting said first logical processor has failed would improve the data integrity of Hays and Dekoning's system with relative ease when any processor fails during its execution of a Perform Locked Operation.

Conclusion

39. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Camquy Truong whose telephone number is (571) 272-3773. The examiner can normally be reached on 8AM – 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-3756.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR of Public PAIP. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIP system, contact the Electronic Business Center (EBC) at 866-217-9197(toll-free).

Camquy Truong

February 7, 2005

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